PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 7,257,015	)	Serial No. 10/621,357
	)	
Inventor(s): Takashi OHSAWA	)	Filed: July 18, 2003
	)	
Issue Date: August 14, 2007	)	Attorney Docket No. 002372.00044

For: SEMICONDUCTOR MEMORY DEVICE HAVING A FLOATING STORAGE BULK REGION

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. A copy of PTO Form 1050 is appended. The complete Certificate of Correction involves one page.

The mistakes identified in the appended Form occurred through no fault of the Applicant, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience are the relevant portions of the Terminal Disclaimer filed May 7, 2007 and the Amendment filed September 5, 2006.

Issuance of the Certificate of Correction containing the corrections is respectfully requested. Since these changes are necessitated through no fault of the Applicant, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: March 18, 2008
Banner & Witcoff, Ltd
1100 13th Street, N.W., Suite 1200
Washington, D.C. 20005-4051
(202) 824-3000

By: /Jordan N. Bodner/
Jordan N. Bodner
Registration No. 42,338

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,257,015

DATED: August 14, 2007

INVENTOR(S): Takashi OHSAWA

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, Notice section (*):
Please insert: --This patent is subject to a Terminal Disclaimer.--

In Column 37, Claim 10, Lines 8 and 11:
Please replace "form" with --formed--

In Column 37, Claim 10, Line 10:
Please replace "transistor" with --transistors--

In Column 37, Claim 10, Line 18:
Please replace "line;" with --lines;--

In Column 37, Claim 10, Lines 24 and 26:
Please replace "carries" with --carrier--

In Column 38, Claim 15, Line 5:
Please replace "the line" with --the word line--

In Column 38, Claim 18, Line 27:
Please replace "the line" with --the word line--

In Column 38, Claim 19, Line 33:
Please replace "of a word" with --of the word--

Mailing Address of Sender:

Banner & Witcoff, Ltd.
1100 13th Street, N.W., Suite 1200
Washington, DC 20005-4051

No. of add'l copies
@ $0.50 per page

PTO/SB/28 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 002372.00044

In re Application of: Takashi OHSAWA

Application No. 10/621,357

Filed: July 18, 2003

For: Semiconductor Memory Device and Method of Manufacturing the Same

The owner*, Kabushiki Kaisha Toshiba, of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term prior patent No. 6,621,725 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney of record. Reg. No. 28,176

/Joseph M. Potenza/ March 7, 2007
Signature Date

Joseph M. Potenza
Typed or printed name

202-824-3000
Telephone Number

☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner). Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Acknowledgement Receipt

EFS ID:	1184588
Application Number:	10621357
Confirmation Number:	2565
Title of Invention:	SEMICONDUCTOR MEMORY DEVICE HAVING A FLOATING STORAGE BULK REGION
First Named Inventor:	Takashi Ohsawa
Customer Number:	22907
Filer:	Jordan N. Bodner
Filer Authorized By:	
Attorney Docket Number:	002372.00044
Receipt Date:	05-SEP-2006
Filing Date:	18-JUL-2003
Time Stamp:	10:54:20
Application Type:	Utility
International Application Number:	

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		00237200044_replacement_listing_of_claims.pdf	117423	yes	9

	Multipart Description		
	Doc Desc	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	9
Warnings:			
Information:			
	Total Files Size (in bytes):	117423	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Atty. Docket No.:	002372.00044
Takashi OHSAWA			
Serial No.:	10/621,357	Group Art Unit:	2824
Filed:	July 18, 2003	Examiner:	Andrew Q. Tran
For:	SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME	Confirmation No.:	2565

REPLACEMENT LISTING OF CLAIMS

U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

In response to the Notice of Non-Compliant Amendment mailed August 3, 2006, Applicant submits herewith a replacement "Listing of Claims."

Since the present paper is filed within one month of the above-mentioned Notice (September 3 and 4 being a Sunday and a federal holiday, respectively), and since the previous Office Action was non-final, it is believed that this paper is timely and no fee is due. Nevertheless, please charge any fees that are due to our Deposit Account No. 19-0733, and any extensions of time needed for acceptance of this paper are hereby requested.

35. (Currently Amended) ~~The semiconductor memory device according to claim 32,~~ A semiconductor memory device, comprising:

an SOI substrate in which a silicon layer is formed on an insulating film formed on a silicon substrate;

a plurality of transistors which have drain diffusion regions and source diffusion regions formed in the silicon layer and gate electrodes formed on the silicon layer, wherein pairs of the transistors, each pair sharing one of the drain diffusion regions, being arranged in a matrix form and element-isolated in a channel width direction, wherein the gate electrodes of the transistors arranged in a first direction are continuously formed so as to form word lines; and

a plurality of bit lines running in a second direction intersecting the first direction and connected to the drain diffusion regions of the transistors;

wherein each of the transistors has a first data state having a first threshold voltage in which excessive majority carriers are held in the silicon layer and a second data state having a second threshold voltage in which the excessive majority carriers in the silicon layer are emitted,

wherein a sense amplifier is provided for the plurality of bit lines, one of the bit lines being selected to be connected to the sense amplifier, and

wherein the first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in the silicon layer, and the second data state is a state in which a forward bias is applied between the silicon layer and the drain diffusion region to extract the excessive majority carriers from within the silicon layer to the drain diffusion region.

36. (Currently Amended) The semiconductor memory device according to claim ~~32~~35, wherein the silicon layer is a p-type, and the transistor is an N-channel MOS transistor.

37. (Currently Amended) The semiconductor memory device according to claim ~~32~~35, wherein a voltage of the source diffusion regions is constant.

38. (Currently Amended) The semiconductor memory device according to claim 37, wherein when data is written, with the source diffusion regions as a reference voltage,

a first voltage higher than the reference voltage is given to ~~a~~ the word line of ~~the a~~ selected ~~transistor~~one of the transistors,

a second voltage lower than the reference voltage is given to ~~a~~ the word line of ~~the~~ a non-selected ~~transistor~~one of the transistors,

a third voltage higher than the reference voltage is given to the bit line when the first data state is written, and

a fourth voltage lower than the reference voltage is given to the bit line when the second data state is written.

39. (Previously Presented) The semiconductor memory device according to claim 38, wherein when the data is read, with the source diffusion regions as the reference voltage, a fifth voltage, which is between the first threshold voltage and the second threshold voltage and higher than the reference voltage, is given to the word line of the selected transistor to detect whether the selected transistor conducts.

40. (Previously Presented) The semiconductor memory device according to claim 38, wherein when the data is read, with the source diffusion regions as the reference voltage, a fifth voltage, which is higher than the first and second threshold voltages and higher than the reference voltage, is given to the word line of the selected transistor to detect a conductivity of the selected transistor.

41. (Currently Amended) The semiconductor memory device according to claim ~~32~~35, wherein when the data is read, after a voltage of ~~a~~ the word line of ~~the~~ a selected ~~transistor~~ one of the transistors is raised more than the second threshold voltage, a predetermined current is supplied to ~~a~~ the bit line of the selected transistor to detect a potential difference in the bit line thereof.

42. (Currently Amended) The semiconductor memory device according to claim ~~32~~35, wherein when the data is read, after a voltage of ~~a~~ the word line of ~~the~~ a selected ~~transistor~~ one of the transistors is raised more than the second threshold voltage, a current is supplied to ~~a~~ the bit line of the selected transistor to clamp the voltage thereof at a predetermined voltage and to detect a difference in the supplied current.

43. (Currently Amended) The semiconductor memory device according to claim 38, wherein when the data is read, after a voltage of ~~a~~ the word line of ~~the~~ a selected ~~transistor~~ one of the transistors is raised more than the second threshold voltage, a predetermined current is supplied to ~~a~~ the bit line of the selected transistor to detect a potential difference in the bit line thereof.

44. (Currently Amended) The semiconductor memory device according to claim 38, wherein when the data is read, after a voltage of ~~a~~ the word line of ~~the~~ a selected ~~transistor~~ one of the transistors is raised more than the second threshold voltage, a current is supplied to ~~a~~ the bit line of the selected transistor to clamp the voltage thereof at a predetermined voltage and to detect a difference in the supplied current.